HIGH-SPEED MASH SIGMA-DELTA MODULATOR ARCHITECTURE AND METHOD OF OPERATION THEREOF

ABSTRACT OF THE DISCLOSURE

A sigma-delta modulator, a method of performing sigma-delta modulation and an digital-to-analog converter incorporating the modulator or the method. In one embodiment, the sigma-delta modulator includes: (1) a lower-order accumulator chain configured to process only lower-order bits of an input number, (2) a higher-order accumulator chain configured to process only higher-order bits of the input number and (3) a combiner coupled to both the lower-order and higher-order accumulator chains and configured to align results therefrom to generate output bits of a given order.